5. (THREE TIMES AMENDED) The circuit according to claim 12, wherein said one or more clock signals each have an impedance that [can be] is adjusted to match an external impedance.

7. (THREE TIMES AMENDED) The circuit according to claim 12, wherein said reference clock frequency is selected from [one] two or more reference clock frequencies in response to (i) a multiplexer and (ii) a configuration signal.

8. (THREE TIMES AMENDED) The circuit according to claim 7, wherein said [one] two or more reference clock frequencies are generated internally to said device.

9. (THREE TIMES AMENDED) The circuit according to claim 7, wherein said [one] two or more reference clock frequencies are generated externally to said device.

22. (AMENDED) A device comprising:

means for implementing programmable logic for manipulating information to generate one or more control signals, wherein said means for implementing programmable logic [configuring] receives one or more clock signals; and

means for generating said one or more clock signals in response to (i) a reference clock and (ii) said one or more control

signals, wherein said one or more clock signals are each capable of oscillating at a different one of a plurality of frequencies, said means for implementing programmable logic [manipulating] and said means for generating are integrated on a single circuit.

2024. (AMENDED) The device according to claim ~~23~~ 19, wherein said one or more clock signals each have an impedance that [can be] is adjusted to match an impedance of an external device.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a device comprising a programmable logic circuit and a phase lock loop circuit. The programmable logic circuit may be configured to (i) generate one or more control signals and (ii) receive one or more clock signals. The phase lock loop circuit may be configured to generate the one or more clock signals, each capable of oscillating at a different one of a plurality of frequencies. The clock signals may be generated in response to (i) a reference clock and (ii) the one or more control signals. The programmable logic circuit and the phase lock loop circuit may be integrated on a single circuit.